## IN THE CLAIMS

Please amend the claims as follows. Please add claims 22-24.

1. (Original) A memory comprising:

$2^n$ dynamic random access memory (DRAM) banks, wherein $n$ is an integer greater than or equal to 2;

$2^n$ refresh row address counter circuits each configured to generate a set of refresh row address signals in response to $2^n$ refresh enable signals;

a multiplexer circuit configured to provide the sets of refresh row address signals to the $2^n$ DRAM banks in response to the $2^n$ refresh enable signals; and

a bank select circuit configured to provide $2^n$ bank enable signals to the $2^n$ DRAM banks in response to at least $(n + 1)$ external address signals and in response to the $2^n$ refresh enable signals;

wherein the $2^n$ bank enable signals cause at least two but less than all of the $2^n$ DRAM banks to be refreshed using at least two of the sets of refresh row address signals in response to the $2^n$ refresh enable signals.

2. (Original) The memory of claim 1 further comprising:

a control circuit configured to generate the $2^n$ refresh enable signals and configured to provide the $2^n$ refresh enable signals to the $2^n$ refresh row address counter circuits, the multiplexer circuit, and the bank select circuit.

3. (Original) The memory of claim 2 wherein the control circuit is configured to generate the $2^n$ refresh enable signals to cause an auto refresh operation to be performed.

4. (Original) The memory of claim 1 wherein the at least $(n + 1)$ external address signals comprise $n$ external bank address signals and at least one external row address signal.

5. (Currently amended) The memory of claim 4 wherein the multiplexer circuit is configured to receive a plurality of external row address signals that include the at least one external row address signal.

6. (Original) The memory of claim 1 wherein the multiplexer circuit comprises $2^n$ multiplexers, wherein each of the $2^n$ multiplexers is configured to receive a plurality of external row address signals and one of the $2^n$ sets of refresh row address signals, and wherein each of the $2^n$ multiplexers is configured to provide one of the $2^n$ sets of refresh row address signals to one of the $2^n$ DRAM banks in response to the $2^n$ refresh enable signals.

7. (Original) The memory of claim 1 wherein each of the $2^n$ DRAM banks comprises a bank row address latch and decoder and a bank cell array.

8. (Original) The memory of claim 1 wherein the at least two of the $2^n$ sets of refresh row address signals provide different values to the at least two but less than all of the $2^n$ DRAM banks at a given time in response to the $2^n$ refresh enable signals.

9. (Original) A system comprising:

a dynamic random access memory (DRAM) comprising:

*n* bank address inputs;

*m* row address inputs;

$2^n$ banks; and

$2^n$ refresh row address counters;

wherein *n* is a first integer greater than or equal to 2, and wherein *m* is a second integer greater than or equal to 2; and

a memory controller configured to generate a bank selector value associated with an auto refresh operation and configured to initiate the auto refresh operation to cause at least two of the banks to be refreshed using at least two of the refresh row address counters by providing the

bank selector value to the DRAM using the *n* bank address inputs and at least one of the *m* row address inputs.

10. (Original) The system of claim 9 wherein the memory controller is configured to perform a read or write operation to one or more of the banks other than the at least two banks being refreshed during the auto refresh operation.

11. (Original) The system of claim 9 wherein the memory controller is configured to perform a bank active or a precharge operation to one or more of the banks other than the at least two banks being refreshed during the auto refresh operation.

12. (Original) The system of claim 9 wherein the memory controller is configured to provide an auto refresh command associated with the auto refresh operation to the DRAM along with the bank selector value.

13. (Original) The system of claim 12 wherein the memory controller is configured to provide a read or a write command to the DRAM subsequent to providing the auto refresh command to the DRAM and prior to completing the auto refresh operation.

14. (Original) The system of claim 12 wherein the memory controller is configured to provide a bank active or a precharge command to the DRAM subsequent to providing the auto refresh command to the DRAM and prior to completing the auto refresh operation.

15. (Original) The system of claim 9 wherein the DRAM comprises synchronous DRAM (SDRAM).

16. (Original) The system of claim 9 wherein each of the at least two refresh row address counters provide different refresh row address values to the at least two banks at a given time.

17. (Original) A method of performing an auto refresh operation in a dynamic random access memory (DRAM) that includes $2^n$ banks where $n$ is an integer greater than or equal to 2, the method comprising:

receiving an auto refresh command;

receiving a bank selector value that designates at least two but less than all of the banks; and

refreshing the banks designated by the bank selector value.

18. (Original) The method of claim 17 further comprising:

performing a operation to a bank not designated by the bank selector value while refreshing the banks designated by the bank selector value.

19. (Original) The method of claim 17 further comprising:

receiving the bank selector value using $n$ bank address inputs and at least one row address input.

20. (Original) The method of claim 17 further comprising:

generating a bank select signal for each of the designated banks using the bank selector value.

21. (Original) The method of claim 17 further comprising:

refreshing the banks designated by the bank selector value using one of a plurality of sets of refresh row addresses for each of the designated banks.

22. (New) A memory comprising:

$2^n$ dynamic random access memory (DRAM) banks, wherein $n$ is an integer greater than or equal to 2;

$2^n$ refresh row address counter circuits each configured to generate a set of refresh row address signals in response to $2^n$ refresh enable signals;

a multiplexer circuit configured to provide the sets of refresh row address signals to the $2^n$ DRAM banks in response to the $2^n$ refresh enable signals;

a bank select circuit configured to provide $2^n$ bank enable signals to the $2^n$ DRAM banks in response to at least $(n + 1)$ external address signals and in response to the $2^n$ refresh enable signals; and

a control circuit configured to generate the $2^n$ refresh enable signals and configured to provide the $2^n$ refresh enable signals to the $2^n$ refresh row address counter circuits, the multiplexer circuit, and the bank select circuit;

wherein the $2^n$ bank enable signals cause at least two but less than all of the $2^n$ DRAM banks to be refreshed using at least two of the sets of refresh row address signals in response to the $2^n$ refresh enable signals, and wherein the at least two of the $2^n$ sets of refresh row address signals provide different values to the at least two but less than all of the $2^n$ DRAM banks at a given time in response to the $2^n$ refresh enable signals.

23. (New) The memory of claim 22 wherein the at least $(n + 1)$ external address signals comprise $n$ external bank address signals and at least one external row address signal.

24. (New) The memory of claim 23 wherein the multiplexer circuit is configured to receive a plurality of external row address signals that include the at least one external row address signal.